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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/720,764

11/25/2003

Masashi Yonemaru

829-618

3114

23117 7590 03/04/2005

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EXAMINER

DICKEY, THOMAS L

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No. 10/720,764	Applicant(s) YONEMARU, MASASHI	
	Examiner Thomas L. Dickey	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 January 2005.
 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
 4a) Of the above claim(s) 2,3,5,7 and 9-23 is/are withdrawn from consideration.
 5) ☐ Claim(s) _____ is/are allowed.
 6) ☐ Claim(s) 1,4,6 and 8 is/are rejected.
 7) ☐ Claim(s) _____ is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some * c) ☐ None of:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/25/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. The preliminary amendment filed on 07/06/98 has been entered.

Election/Restriction

2. Applicant's election without traverse of Embodiment 2 (the species of Figs. 8A-8B and 9A-9C and page 53, line 3 through page 56, line 13) claims 1, 4, 6 and 8 in the Paper filed 01/24/2005 is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 03/22/2004 is acceptable.

Drawings

4. The formal drawings filed on 03/22/2004 are acceptable.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

6. The Information Disclosure Statement filed on 11/25/2003 has been considered.

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Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,4,6, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Taki (6,329,845).

Taki discloses a semiconductor integrated circuit, comprising a first cell 2 (the first cell 2 is most easily identified in figure 50) comprising a plurality of transistors including a PMOS transistor (the upper of the two transistors in cell 2, as seen in figure 50) and an NMOS transistor (the lower of the two transistors in cell 2, as seen in figure 50); a second cell 1 (the second cell 1 is most easily identified in figure 50) comprising a PMOS transistor section, the PMOS transistor section comprising a first PMOS transistor (the first PMOS transistor is most easily seen in figure 50, as the uppermost of the four transistors on the left hand side of cell 2. Its source is connected to first source voltage Vdd, and its gate is connected to input signal A, in figure 50) and a second

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PMOS transistor (the second PMOS transistor is most easily seen in figure 50, as the second uppermost of the four transistors on the left hand side of cell 2. Its source is connected to the drain of the first PMOS transistor, and its gate is connected to first gate control signal D, in figure 50), each comprising a gate, a source, and a drain (note figure 47A) the first and second PMOS transistors being connected in series; and an NMOS transistor section, the NMOS transistor section comprising a first NMOS transistor (the first NMOS transistor is most easily seen in figure 50, as the lowermost of the four transistors on the left hand side of cell 2. Its source is connected to second source voltage GND, and its gate is connected to input signal A, in figure 50) and a second NMOS transistor (the second NMOS transistor is most easily seen in figure 50, as the second lowermost of the four transistors on the left hand side of cell 2. Its source is connected to the drain of the first NMOS transistor, and its gate is connected to second gate control signal B, in figure 50), each comprising a gate, a source, and a drain (note figure 47A), the first and second NMOS transistors being connected in series.

Taki further discloses that a predetermined scheme is used to connect between the first cell 2 and the second cell 1, between the plurality of transistors in the first cell 2, and between the PMOS transistor section and the NMOS transistor sections in second cell 1, that first cell 2 functions as a logic operation circuit (logical "NOT," note figure 49B) for outputting data and second cell 1 functions as at least one of a driver circuit (circuit AOI22, note figure 49B) for driving the logic operation circuit, that a first source

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voltage Vdd (note figure 50) is applied to the source of the first PMOS transistor, a second source voltage GND (note figure 50) is applied to the source of the first NMOS transistor, that one of the gate of the first PMOS transistor and the gate of the second PMOS transistor, namely, the gate of the first PMOS transistor, is connected to an input terminal (input terminal "A," seen in figure 47A), the other, namely, the gate of the second PMOS transistor, is connected to a first gate control signal input terminal (input terminal "D," seen in figure 47A), a first gate control signal (first gate control signal D, note figure 50) being input to the first gate control signal input terminal "D," one of the gate of the first NMOS transistor and the gate of the second NMOS transistor, namely, the gate of the first NMOS transistor, is connected to input terminal "A," and the other, namely, the gate of the second NMOS transistor, is connected to a second gate control signal input terminal (input terminal "B," seen in figure 47A), a second gate control signal (second gate control signal B, note figure 50) being input to the second gate control signal input terminal "B," and (note, figure 50, that the drains of the second PMOS and second NMOS transistors are connected together) the drain of the second PMOS transistor and the drain of the second NMOS transistor are connected (via first cell 2) to output terminal Y (again, please note figure 50). Note figures 47A-B, 48A-B, 49A-B, and 50, and column 14 lines 48-67 of Taki.

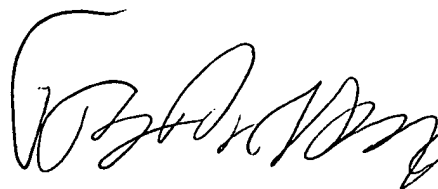
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Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
03/05